PROCESS-VOLTAGE-TEMPERATURE VARIATION DETECTION AND CANCELLATION USING ON-CHIP PHASE-LOCKED LOOP

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Abstract –*A study of a PVT compensation method based on an external reference clock is presented. A compensation mechanism integrated into the system PLL is developed and studied, its effectiveness has been assessed for analogue systems. The proposed method has been tested on a classical charge-pump PLL, showing adequate PVT compensation and improved jitter and power consumption performance as a result.*

1. INTRODUCTION

Process, voltage and temperature (PVT) variation of key parameters in integrated circuit (IC) components has always been an important problem [1, 2]. Keeping up with Moors law, by constantly shrinking the characteristic dimensions of IC components makes this problem demanding more and more attention. In deep submicron processes variation of transistor threshold voltage can go over 30%, sheet resistance variation of poly-silicone resistors reaches 40% for some technologies. Variation of device parameters inevitably results in variation of overall circuit parameters, affecting its performance, power consumption as well as decreasing the yield. PVT variation effects are especially pronounced in high speed systems, where requirements on performance parameters are stringent. This imposes a need for PVT variation detecting and subsequent compensation means to be developed.

Classical bandgap references [3] can provide sufficient temperature compensation only for voltage leaving the problem of on-chip current compensation unsolved. Adequate compensation can be achieved in systems using external (off-chip) resistors, similarly to DDR IO. However external devices are considered an unwanted measure for commercial reasons.

An alternative compensation method, using external reference clock is proposed. Precise reference signals are available for most of modern high speed data-systems. A compensation solution integrated into system phase locked loop (PLL) is considered. Its efficiency of PVT compensation of PLL itself and system overall was studied here. Noticeable improvement of circuit performance has been achieved in expense of increased area and overall complexity.

2. PVT VARIATION AND ITS EFFECTS ON HIGH-SPEED SYSTEMS

As technologies move deeper into sub-micron the manufacturing process non-ideality becomes more pronounced, causing threshold voltage V_{th}, gate thickness and hence oxide capacitance C_{ox} as well as other device key parameter deviations from target (typical) values.

Die temperature constantly changes depending on ambient temperature and IC power dissipation induced heating. Temperature drift manifests itself in transistor threshold voltage and carrier mobility deviations.

Supply voltage is also subject to unwanted fluctuations over time.

The mentioned effects usually have adverse effects on high speed system performance. As an example of such a system a charge pump PLL is considered. Voltage controlled oscillator (VCO), Fig.1, is especially vulnerable to PVT fluctuations [2, 4]. A simple 5-stage differential VCO with controlled delay cell depicted in Fig.2 was used.

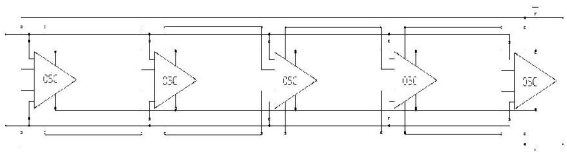

Fig.1. *5-stage voltage controlled oscillator*

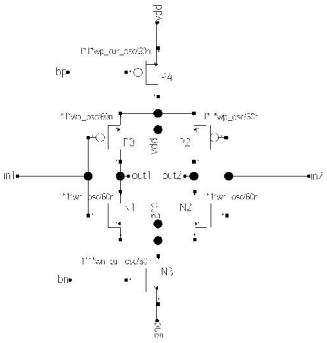

Fig.2. *VCO differential delay cell*

For the VCO output frequency the following expression takes place, if biasing circuit is designed correctly:

$$F_{vco} \sim \frac{I_{tail}}{2 * C_n * N * V_{swg}}, \qquad (1)$$

where F_{vco} is the output frequency, I_{tail} is the tail current source current; C_n is the total capacitance at the VCO delay stage output, N is the number of stages and V_{swg} voltage swing in the VCO output. For saturated current tails:

$$I_{tail} \sim k(V_{gs} - V_{th})^2 * (1 + \lambda * V_{ds}), \qquad (2)$$

where:

$$V_{gs} = V_{dd} - V_{bp} = f(V)$$
$$V_{th} = f(\mathrm{P},\mathrm{T}) \quad . \quad (3)$$
$$C_n = f(\mathrm{P})$$

Here V_{gs} is a function of supply voltage, V_{th} is a function of process and temperature and C_n is a function of the process. Compensating these variations separately is not feasible on practice. However F_{vco} can be effectively compensated if a mechanism for I_{tail} current calibration, depending on F_{vco} variation, exists. This concept is used in this paper.

1. Compensating currents in VCO bias circuit helps keep its central frequency control voltage V_{c0} stable hence allowing to operate in the linear region of $f(V_c)$ characteristic, Fig.3. This is essential for input noise to be prevented from propagating into higher harmonics due to nonlinearity effects [2].

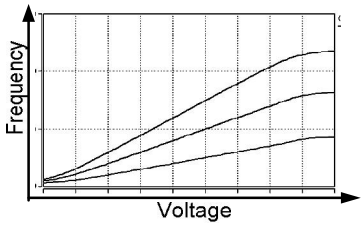

Fig.3. *VCO frequency V.S. control voltage for different process corners*

2. Compensated bias currents keep VCO gain [2, 4] stable. The gain increase due to PVT changes, increases VCO sensitivity to the noise contained in the control signal. This increases the output jitter, Fig.3.

3. The increase of currents in the cells that share the same supply voltages with VCO (ex. PLL other components) results in growth of noise at supply rails. This induces significant jitter in VCO. The amplitude of supply rail noise depends on the package L inductance, R resistance of the rails and decoupling capacitance between the mentioned rails. Fig.4 shows dependence of a typical PLL period jitter on the average switching current of neighbouring cells and decoupling capacitance. As it can be seen, it is important to prevent switching current increase due to PVT changes in order to keep jitter low for the given amount of decoupling devices.

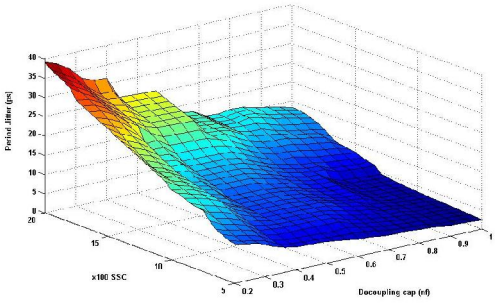

Fig.4. *Output jitter dependence on average switching current and supply decoupling capacitance*

3. PROPOSED PVT DETECTION MECHANISM

For proper PVT compensation to be achieved a detection circuit is necessary. Detection circuit operation is based on an on-die PVT dependent parameter comparison to a similar reference parameter. The primary requirement imposed on the reference parameter is the stability. Of the chip reference clock frequency can be used in the mentioned role due to its stability and availability in majority of data-systems. An on-die VCO output frequency is used as a PVT variable. Block diagram of the detection circuit is shown in Fig.5. The system consists of a VCO as a part of the on-die PLL, and register transfer logic (RTL) block.

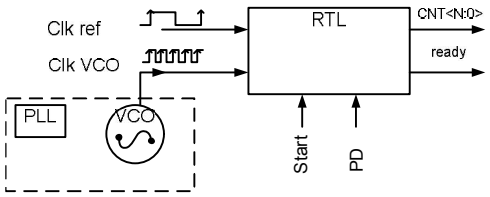

Fig.5. *Blok diagram of the PVT sensing circuit*

RTL block is responsible for comparing VCO output clock f_{cvco} to the reference clock f_{ref} and producing a code corresponding to the frequency. Knowing the frequency code under typical conditions allows making judgements about frequency deviations with precision sufficient for most of the analogue and mixed mode systems. Fig.6. shows simplified timing diagrams for the described compensatory mechanism.

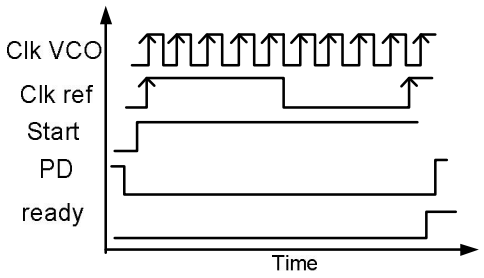

Fig.6. *Simplified timing diagram*

When RTL start input is asserted and PD (power down) de-asserted detection starts with the reference clock positive transition (posedge), the system counts VCO clock cycles (posedges) until the second posedge transition of the reference. Second transition signifies completion of detection process, asserting "ready" output high and producing "CNT" code in the output. Each value of the code corresponds to a specific VCO frequency. CNT code can be produced in different encodings depending on the specifics of a system. Thermometer encoding is considered in this paper.

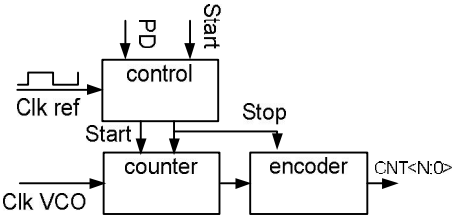

Fig.7. *RTL block diagram*

The RTL block in Fig.7 consists of a controller, main counter and encoder sub-blocks. The controller is responsible for detection activation/deactivation depending on start and reference clock signals. Counter counts VCO clocks if PD is released and start command from controller received. The encoder translates data received from the counter into the required encoding format and produces 'ready' signal after operation is completed.

To characterize the ability of the described circuit to detect PVT changes a simple concept of resolution is introduced.

$$R_S = \frac{T_{ref}}{T_{c0}}, \tag{4}$$

where T_{ref} is the reference clock period time and T_{c0} is VCO clock period. In fact, VCO period should change by some ΔT amount to be successfully detected by the system.

For the circuit described in Fig.5, the following expression takes place:

$$T_{ref} = N * T_{c0}, \tag{5}$$

if, due to some reason, VCO frequency changes to T'; where $T'=T_{c0} + \Delta T$. using (5) and considering T_{ref} constant the following expression can be achieved:

$$N * T_{c0} = (N+1) * T', \tag{6}$$

or

$$\frac{N}{(N+1)} = 1 + \frac{\Delta T}{T_0}. \tag{7}$$

Considering (7) the following expression for ΔT can be written:

$$\left|\Delta T\right| = \frac{\frac{T_{c0}}{T_{ref}}}{1 + \frac{T_{c0}}{T_{ref}}} * T_{c0}. \tag{8}$$

Substituting (4) in (8) brings to:

$$\left|\Delta T\right| = \frac{\frac{1}{Rs}}{1 + \frac{1}{Rs}} * T_{c0} \xrightarrow[Rs\to\infty]{} 0. \tag{9}$$

This expression proves the logical conclusion that for high precision detection VCO frequency must be significantly higher than that of the reference clock. However excessively high precision is not always desirable since it requires high complexity of counter and encoder as well as correspondingly complicated PVT compensation circuitry. All this can result in unacceptably high area and complexity increase. The optimal ΔT should be defined considering specifics of the system. The RTL block can be modified to limit the resolution if $T_{ref} >> T_{c0}$.

4. PVT COMPENSATION MECHANISM

PVT compensation is achieved through compensating circuit currents in the system. Feasibility of effective compensation is suggested by the formula (1), where VCO tail source currents are in proportional relationship with the frequency. Even though C_n and V_{swg} are variables of process and voltage variations, they introduce relatively small variation (<10%) [2, 4, 5]. Most of the frequency variation results from the current changes.

The PVT detection circuit thermometer code contains information about the variation of the VCO frequency with respect to the typical frequency. The proportional relationship between current and frequency allows using frequency variation code to adjust the current. For example, if the detection code suggests increase of frequency by some factor *m*, then the decreasing current in (1) by the same factor will restore the frequency with high precision. Compensated current can be used not only in VCO itself but for other system components, including PLL sub-blocks, employing similar current biasing as VCO.

Fig.8. shows the simplified diagram for PVT detection and compensation in a classical charge pump PLL.

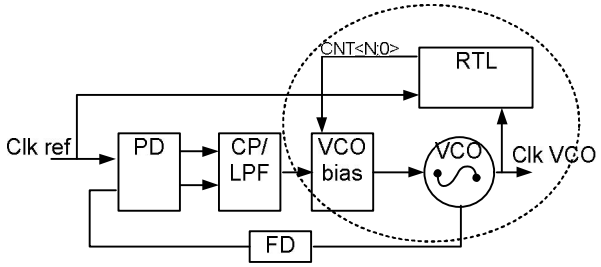

Fig. 8. *PVT detection and compensation in a PLL*

The PLL is deactivated during the detection process, all its components are powered down and VCO input (control voltage) connected to voltage corresponding to typical conditions (e.g. Vdd/2). The PVT detection process is carried out as described in the section 3, and a corresponding PVT code is generated and stored. The PVT code is applied to digitally controlled bias generators, which, in simplest case with thermometer code are digitally controlled current mirror array based solutions. After recalibration of reference current values, the detection circuit is deactivated and PLL enters its normal operation mode.

While the process calibration in essence needs to be done only once, the temperature and voltage calibration may need to be recalibrated over time. Depending on the architecture of a system, the detection and compensation can be performed in online mode or in some system defined periods of time.

The described compensation method can effectively stabilize circuit currents, decreasing maximal power consumption, switching activity of supply rails and, hence, power supply induced noise. Moreover it helps avoid overdesigning to achieve adequate performance in slow corners, sacrificing some power and timing margins in typical and fast corners.

5. SIMULATION RESULTS

The reference clock based PVT detection and compensations method was tested on a classical 5 GHz PLL with 100MHz stable reference clock in its input. Simulations were performed with Hspice [6] analogue simulator in a 45nm technology.

To determine susceptibility of VCO to variation as well as to obtain frequency values for in main PVT corners, it was simulated standalone (PLL deactivated) over 27 PVT corners, see Table.1.

Table 1. *Simulation results for VCO in different PVT conditions*

Temp.	Voltage	TT	FF	SS
-40	max	6,16	7,27	5,25
25	max	5,79	6,53	4,76
125	max	5,25	6,16	4,35
-40	min	4,40	5,40	3,27
25	min	4,15	5,14	3,35
125	min	3,96	4,84	3,12
-40	typ	5,40	6,35	4,34
25	typ	5	6,02	4,11
125	typ	4,64	5,53	3,76

TT, FF and SS are respectively typical, fast and slow process variation corners. As it is seen from the table, for fast and slow corners there is over 50% frequency variation from the typical corner. In 5 GHz VCO the resolution R_s=50 which is sufficient to detect effectively frequency deviations as low as about 0.2GHz. The frequency detecting method can also be very useful for comparing simulation results for different PVT conditions with the results from real silicon.

The efficiency of the compensating mechanism was tested in terms of decreasing power consumption and output jitter, through decreasing switching current induced ripple at the supply rails. Power consumption was measured for locked PLL in 3 PVT corners for both compensated and non-compensated cases respectively. Fig.9 compares power (in mW) results for compensated/uncompensated cases.

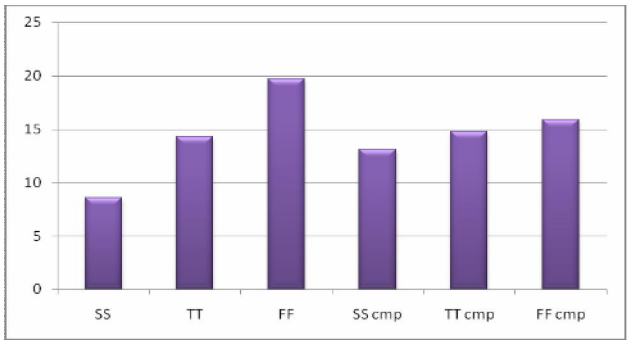

Fig. 9. *Comparison of consumed power variation for compensated/uncompensated PLL*

While there is about 39% power variation in uncompensated circuit, this variation drops to ~11% after calibration of currents is performed.

Stabilization of switching currents has positive effects on voltage supply induced noise. This noise is especially pronounced in fast PVT corners as well as highly depends on temperature and supply voltage. Simulations of the PLL in locked state for compensated/uncompensated cases have shown decrease of overall jitter by up to 17% in fast corners.

The main drawback of the suggested mechanism is the increase of circuit area due to comparatively large detection RTL blocks and compensating current biasing added. For a compensated PLL only the area increase can reach up to ~25 however for complex data systems the resulting increase in percentage will be much lower. Increase of the circuit complexity can also be considered a drawback in some cases.

6. CONCLUSIONS

A simple and efficient PVT variation detection and compensation mechanism was presented. The considered architecture is based on local oscillator frequency comparison with the external precise reference clock frequency. A code obtained from comparison is used to modify bias currents correspondingly, keeping power and timing performance stable. In order to assess the efficiency of the suggested solution an self compensated 5-GHz CMOS PLL was designed. The PVT compensation decreased power consumption variation by as much as 28%. Compensation also showed improvement of output jitter due to satbilization of VCO gain and decrease of current switching induced power rail noise. Jitter decrease of 17% was achieved. The main drawbacks of the solution are the increased area and overall system complexity.

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